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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Tsuruto Matsui	Group Art Unit 2133
Serial No.	:	09/853,998	
Filed	:	May 12, 2001	
For	:	PATTERN GENERATOR FOR SEMICONDUCTOR TEST SYSTEM	
Examiner	:	Unknown	

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

Enclosed is a form PTO-1449 listing three prior art references relevant to the above-identified application.

These references, U.S. Patent Nos. 6,094,738, 5,852,618 and 6,032,275, are relevant to the invention in the instant case because the semiconductor test system in these patent includes means for inverting test patterns.

Applicant respectfully requests that the references submitted be considered in the substantive examination of this case.

Respectfully submitted,

MURAMATSU & ASSOCIATES

Dated: 9/10/01

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